Very high-cycle fatigue failure in micron-scale polycrystalline silicon films: Effects of environment and surface oxide thickness

D. H. Alsem
Department of Materials Science and Engineering, University of California, Berkeley, California 94720; Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720; and National Center for Electron Microscopy, Lawrence Berkeley National Laboratory, Berkeley, California 94720

R. Timmerman
Department of Applied Physics, University of Groningen, Groningen, The Netherlands 9747AG, The Netherlands

B. L. Boyce
Materials Science and Engineering Center, Sandia National Laboratories, Albuquerque, New Mexico 87185

E. A. Stach
School of Materials Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, Indiana 47907

J. Th. M. De Hosson
Department of Applied Physics, University of Groningen, Groningen, The Netherlands 9747AG, The Netherlands

R. O. Ritchie[a)]
Department of Materials Science and Engineering, University of California, Berkeley, California 94720 and Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720

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Fatigue failure in micron-scale polycrystalline silicon structural films, a phenomenon that is not observed in bulk silicon, can severely impact the durability and reliability of microelectromechanical system devices. Despite several studies on the very high-cycle fatigue behavior of these films (up to 10^{12} cycles), there is still an on-going debate on the precise mechanisms involved. We show here that for devices fabricated in the multiuser microelectromechanical system process (MUMPs) foundry and Sandia Ultra-planar, Multi-level MEMS Technology (SUMMiT V™) process and tested under equi-tension/compression loading at ~40 kHz in different environments, stress-lifetime data exhibit similar trends in fatigue behavior in ambient room air, shorter lifetimes in higher relative humidity environments, and no fatigue failure at all in high vacuum. The transmission electron microscopy of the surface oxides in the test samples shows a four- to sixfold thickening of the surface oxide at stress concentrations after fatigue failure, but no thickening after overload fracture in air or after fatigue cycling *in vacuo*. We find that such oxide thickening and premature fatigue failure (in air) occur in devices with initial oxide thicknesses of ~4 nm (SUMMiT V™) as well as in devices with much thicker initial oxides ~20 nm (MUMPs). Such results are interpreted and explained by a reaction-layer fatigue mechanism. Specifically, moisture-assisted subcritical cracking within a cyclic stress-assisted thickened oxide layer occurs until the crack reaches a critical size to cause catastrophic failure of the entire device. The entirety of the evidence presented here strongly indicates that the reaction-layer fatigue mechanism is the governing mechanism for fatigue failure in micron-scale polycrystalline silicon thin films. © *2007 American Institute of Physics*.
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I. INTRODUCTION

Silicon is the most widely used material for microelectromechanical systems (MEMS) sensors and actuators. This is because silicon can be microfabricated to produce complex mechanical structures in thin-film form because of highly developed processing methods directly related to semiconductor electronics processing.[1,2] However, silicon is not an ideal structural material: it is quite brittle and subject to several reliability concerns—most importantly, stiction,[3,4] wear,[3,5] and fatigue[6–24]—that strongly limit the utility of silicon MEMS devices in commercial and defense applications. In particular, premature fatigue failure can occur when devices are subjected to a large number ($\sim 10^6$–10^{12}) of loading cycles at stress amplitudes well below their monotonic fracture stress. This may arise from vibrations intentionally induced in the structure (e.g., resonators found in radio fre-

[a)]Electronic mail: roritchie@lbl.gov

quency MEMS applications) or due to the service environment (e.g., engine vibration on an air bag deployment accelerometer in a car). Additionally, because the surface-to-volume ratio in these structural films is very large, the traditional failure models that have been developed for materials at the bulk scale cannot always be relied upon to accurately predict behavior, essentially because new physical mechanisms may be operative. Indeed, it is clear that at these length scales, surface effects may become dominant in controlling mechanical properties. While the reliability of MEMS has received extensive attention, the mechanisms responsible for the various failure modes have yet to be conclusively determined. This is particularly true for the fatigue of micron-scale silicon films, a research area that has been the subject of intense debate.[6–24]

Although bulk silicon is not susceptible to fatigue failure in ambient air,[25,26] thin silicon structural films are.[6] In previous studies we proposed that the fatigue of micron-scale polycrystalline silicon (polysilicon) films is a result of a reaction-layer fatigue process,[10–12] whereby high local cyclic stresses induce thickening of the post-release amorphous SiO_2 oxide layer at stress concentrations such as notches. As silica is highly sensitive to environmentally assisted fracture, subcritical (stable) cracking induced by the presence of moisture occurs within the oxide layer to form a crack large enough to fracture the entire device. The mechanism explains why bulk silicon is not susceptible to such fatigue failure, as the subcritical cracks within the oxide layer can never get large enough to cause fracture of the entire structure.

Recently, the reaction-layer fatigue mechanism has been called into question by some researchers,[14–16] who instead proposed a series of alternative mechanisms, all of which are purported to account for the fatigue effect occurring in (polycrystalline) silicon. In these counter arguments, the fatigue damage is suggested to be strongly affected by the compressive portion of the loading cycle, with (i) crack growth due to a mechanism similar to cyclic compression fatigue of notched, brittle ceramic bulk specimens[27] aided by a wedging effect of silicon debris or the oxidized surface inside the crack; or (ii) crack growth occurring by dislocation activity, which causes either crack-tip blunting or crack-tip blunting followed by sharpening (similar to fatigue in ductile materials); or (iii) that grain-boundary deformation by means of shear deformation in the thin amorphous region of a grain boundary hitting the surface causes stable crack growth. All of these suggested mechanisms suffer from the fact that they cannot explain why micron-scale silicon is susceptible to fatigue and bulk silicon is not. More importantly, there is no direct experimental evidence to support these proposed alternative mechanisms. Indeed, the crack growth in compression, associated with debris or surface oxidation induced "cantilever effects," has been largely discounted as a mechanism of tensile fatigue in brittle materials. Pierron and Muhlstein[28] have further shown that such phenomena will not cause an increase in the magnitude of the stress intensity factor at the crack tip. Additionally, our detailed observations have revealed no evidence for asperity contact, dislocation activity under these particular loading conditions, nor of grain-boundary plasticity. Similarly, there have been no reports in the literature of such phenomena. Moreover, since single crystal silicon also displays similar fatigue behavior,[6,8,29,30] universal mechanisms involving grain boundaries are unlikely to be relevant. The purely mechanical alternative mechanisms ignore the role of stress-induced oxide thickening, which has been observed now by several investigators.[11,12,18,22] Furthermore, this brings into question whether the polysilicon films utilized in earlier studies were representative due to their relatively thick post-release oxide scales (typically ~20–30 nm[12] rather than the order of a magnitude smaller native oxide layers expected for polysilicon[31]). Pierron *et al.*,[32] however, have recently shown that the relatively thick post-release oxide layers found in these devices, which were all fabricated in the multiuser MEMS process (MUMPs) foundry,[33,34] arise from a galvanic effect of the n^+-type silicon and gold in concentrated HF during release of the freestanding structures at the end of the fabrication process, a finding that was later confirmed.[35]

In the present work, we have used on-chip testing and a series of transmission electron microscopy (TEM) techniques to further investigate fatigue in micron-scale *n*-type polysilicon MEMS resonators. In light of the discussion[6–24] outlined above concerning the mechanism of such thin-film silicon fatigue, our prime objective is to examine the susceptibility to fatigue of polycrystalline silicon films with much thinner initial oxide layers, specifically fabricated by the Sandia Ultra-planar, Multi-level MEMS Technology (SUMMiT V™) process, and to verify the reproducibility of our previous findings across fabrication runs with respect to fatigue properties and oxide layer thicknesses. Additionally, we characterize the changes in fatigue behavior and the development of reaction layers with environment, in both relatively oxygen-/moisture-free and moisture-rich, high relative-humidity environments, and specifically examine the fatigue susceptibility of polysilicon films with thin initial oxide layers *in vacuo*, where resistance to fatigue would be expected to be the largest.

II. EXPERIMENTAL PROCEDURES

Phosphorous-doped polysilicon fatigue resonator devices from both the MUMPs foundry (fabrication runs 18 and 50)[33,34] as well as the Sandia National Laboratories (SUMMiT V™) process[36] were studied. Both sets of devices, i.e., on-chip fatigue specimens, were fabricated using the same device design originally developed by Van Arsdell and Brown.[37] The device consists of a ~300 μm sized triangularly shaped free-standing proof mass connected to an anchor on the substrate by a notched cantilever beam (see Fig. 1). The mass is electrostatically driven at resonance in plane with fully reversed loading ($R=-1$, where R is the ratio of minimum to maximum stress) by an interdigitated comb drive at one side of the device, whereas the comb structure on the other side of the proof mass is used to capacitively sense the displacement of the device during operation. Using the measured displacement and finite-element calculation methods (ANSYS 5.7), the stress at the notch in the cantilever beam during the test can be readily calculated.

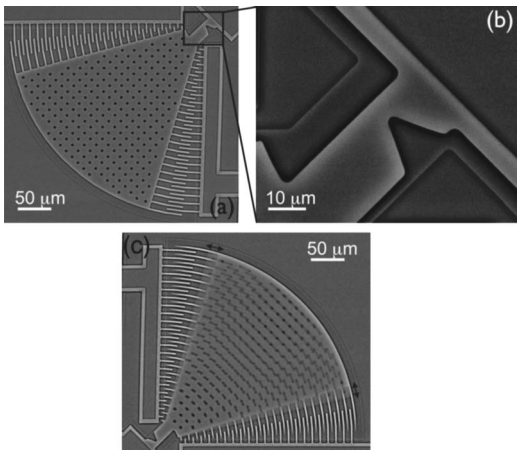

FIG. 1. Scanning electron micrographs of the polysilicon MEMS fatigue life characterization resonator. (a) Triangular free-standing proof mass with interdigited comb drive on one side and capacitive displacement sensor combs on the other side, (b) notched cantilever beam connecting the resonator mass to the anchor, and (c) resonator device operated *in situ* in a scanning electron microscope—in the image the edges of the comb fingers are blurred because of the high frequency motion.

The electrostatic actuation is based on applying a bias across one set of combs in the comb drive. The magnitude of the force (F) created by the drive is given by:

$$F = \varepsilon \frac{nh}{g} V^2,$$

where ε is the dielectric constant of the medium between the comb fingers, n is the number of comb finger, h is the thickness of the comb fingers, g is the gap between the fingers, and V is the applied voltage.[38] When a sinusoidal voltage ($V=A_0 \sin \omega t$) is applied to the comb drive, it can be shown that the magnitude of the resulting force is proportional to $A_0^2 \cos 2\omega t$. Consequently, by applying a sinusoidal voltage at half the resonance frequency, the device can be run at resonance. Capacitive displacement sensing is done by measuring a small current flowing from the opposite set of combs that originates by changing the capacitance of the set of overlapping comb fingers while applying a constant dc voltage. Custom-built electronics, which also filter this signal using an adjustable bandpass filter, convert the current into a voltage that is input into a computer system running LABVIEW. After optically calibrating this voltage with the corresponding displacement, measuring the displacement as a function of the driving frequency allows the fatigue resonator devices to be run at resonance. The resonance frequency and the displacement can be periodically updated during the test by sweeping the frequency and monitoring the displacement. This feedback mechanism allows the displacement to be held constant during the test. Finite-element modeling has shown that a decay in the resonance frequency of the resonators during the test can indicate both cracking as well as oxide formation at the notched cantilever beam.[11]

The n^+-type polysilicon MUMPs devices were fabricated in run 50 of the process and had a structural film thickness of 2 μm and a resonance frequency of approximately 40 kHz. To calibrate the capacitive displacement sensing, this type of device was run in a microvision system[9,18] and *in situ* under a regular optical microscope. The SUMMiT V™ devices came from the five-layer polysilicon process and were n-type polysilicon with structural film thicknesses of 2.25 μm for devices fabricated from layer P3 and 2.5 μm for devices from a stack of layers P1 and P2 (P21). The resonant frequencies are approximately 36 and 37 kHz, respectively, and the calibration of these devices was performed *in situ* under an optical microscope. All devices were packaged in dual inline packages, and ultrasonically bonded aluminum wires were used to connect the package wiring to the contact pads on the MEMS chips.

Using the system described above, experiments were performed in ambient air [25 °C, 30%–40% relative humidity (RH)] for both type of devices and both film thicknesses to determine the applied stress versus total life (S/N) curves. High relative humidity air experiments (~25 °C, >95% RH) were performed on the MUMPs devices in an environmental chamber by bubbling dry air through two water vessels. Both the MUMPs devices as well as the SUMMiT V™ devices have been run in very high vacuum (~25 °C, $<2.0\times10^{-7}$ mbar), although for the SUMMiT V™ devices only the P21 devices were operated *in vacuo*.

Following fatigue testing, the fatigued and fractured beams were imaged using TEM. The MUMPs resonator proof masses were transferred to copper TEM clamshell grids and observed in the unthinned condition in the Berkeley JEOL-JEM 1000 high-voltage electron microscope (HVEM) operated at 800 keV. After thinning using a dual-beam focused-ion beam (FIB) system (FEI Strata DB235 Dual Beam FIB), the SUMMiT V™ devices were imaged in a Philips CM200-FEG, operated at 200 keV, with a Gatan image filter (GIF) system. This allows energy-filtered imaging to create an elemental map of an area of interest [so-called energy-filtered transmission electron microscopy (EFTEM)]. Inside the FIB, a sharp tungsten micromanipulator needle was used to move the fractured resonator masses from the MEMS chip surface to (half) a copper TEM grid by temporarily welding it to the resonator mass with deposited platinum [Figs. 2(a)–2(c)]. A ~100 nm thick carbon layer was sputtered onto some of the samples to assure that the oxide layers would be delineated more clearly. Using standard FIB techniques,[39] the area at the notch was thinned starting from the side of the ligament not containing the notch, after depositing a protective layer of platinum on the same side [Figs. 2(d)–2(f)]. Applying the platinum layer, as well as ion milling from the back of the sample, was necessary to prevent ion implantation during thinning and subsequent damage of the surface.

III. RESULTS

A. *S/N* fatigue results

Figure 3 shows a comparison of the maximum applied cyclic fatigue stress-lifetime (S/N) data for both MUMPs (run 50) and SUMMiT V™ devices, tested in air, high humidity, and high vacuum, along with our previous air data for MUMPs devices (run 18) from Ref. 11. Several trends are apparent in these results, which run out to lifetimes approaching 10^{12} cycles, i.e., on the order of ten months.

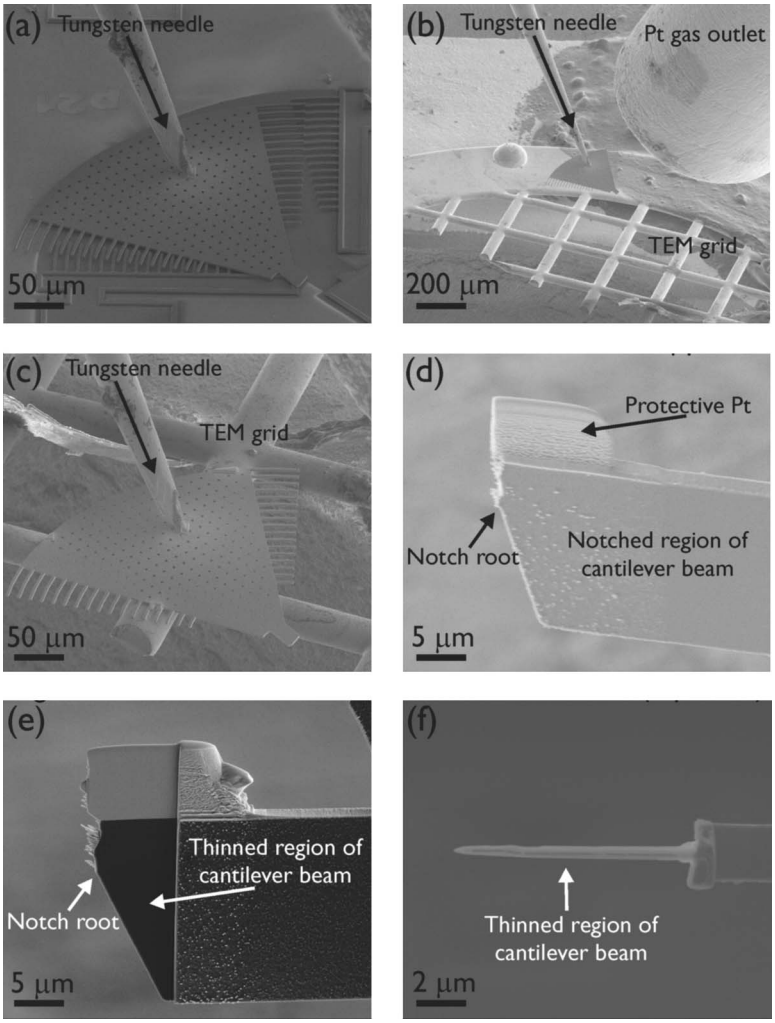

FIG. 2. FIB thinning TEM sample preparation method for SUMMiT V™ devices. (a) Tungsten micromanipulator needle is welded to the fatigued resonator and is lifted above the substrate; (b) the resonator is moved over to the TEM grid; the (c) resonator is Pt welded to the TEM grid; the (d) after removing the needle from the resonator a protective layer of platinum is deposited (some of the samples also had a carbon layer sputtered on top to make the oxides stand out more clearly). [(e) and (f)] An electron transparent thinned sample. The thinned region of the cantilever beam in (e) is perpendicular to the plane of the image in (f).

(1) All curves for tests in air (~25 °C, 30%–40% RH) show typical *S*/*N*-type behavior with lower applied stresses resulting in a larger number of cycles to failure (Fig. 3). Specifically, at stresses of ~70% of the fracture stress, failures occur after some 10^{11} cycles. A close correspondence is seen between the two sets of MUMPs devices, from the earlier fabrication run 18 (Refs. 10 and 11) to the current run 50. Compared to the SUMMiT V™ runs, these devices have lower fatigue resistance.

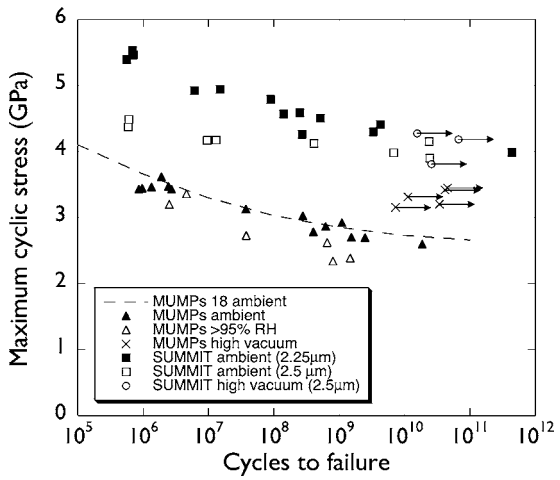

FIG. 3. Combined maximum cyclic stress-lifetime (*S*/*N*) data (at $R=-1$) for polysilicon MUMPs and SUMMiT V™ devices, the last type with two different structural silicon film thicknesses (2.25 and 2.5 μm). Different types of devices are tested in ambient air (~25 °C, 30%–40% RH), high relative humidity (~25 °C, >95% RH), and very high vacuum (~25 °C, $<2.0\times10^{-7}$ mbar). For comparison, a curve fit to fatigue data from MUMPs run 18 by Muhlstein *et al.* (Refs. 10 and 11) is also shown.

(2) The extent of accumulated fatigue damage, which can be primarily associated with oxidation and crack growth and is confirmed by finite-element modeling,[40] was qualified for the SUMMiT V™ samples by monitoring the change in resonance frequency throughout the fatigue tests (Fig. 4). For all tests in air, a monotonic decrease in resonance frequency was observed during the entire fatigue life up until the point of failure, similar to that which was reported previously for the fatigue of the MUMPs devices.[11] A larger total decrease in resonance frequency at the point of failure was found for tests run at lower stress, as shown in Fig. 5. The relation between the number of cycles to failure and total decrease in resonance frequency can be qualitatively compared to the proportionality following the expression for the stress intensity: K is proportional $\sigma\sqrt{a}$, where σ is the stress and a is the crack length. Plotting the number of cycles to failure exponentially (which is proportional to the applied cyclic stress σ, as can be derived from the

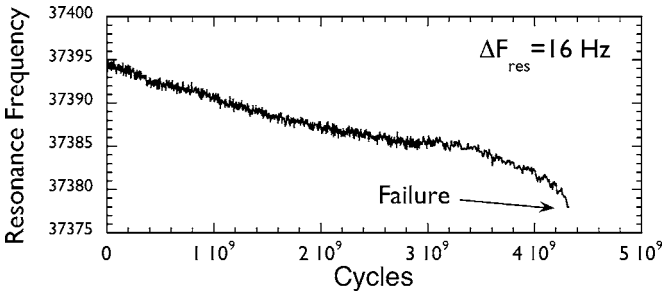

FIG. 4. Typical example of resonance frequency (F_{res}) behavior of SUMMiT V™ devices during fatigue tests. The decrease in resonance frequency (ΔF_{res}), in Hz, with number of cycles throughout the fatigue life is associated with damage accumulation, in the form of oxide growth and subcritical cracking within the oxide layer.

experimental S/N results in Fig. 3) versus the change in resonance frequency (which is proportional to the crack length a, here assumed to be roughly the same size as the thickness of the oxide layer), a (negative) second-order trend is found (Fig. 5). This also shows that the experimental, yet indirect, crack-propagation measurements by monitoring the resonance frequency are consistent with the theoretical expression for the stress intensity reached at failure and therefore give a good indication of damage accumulation in these test samples.

(3) Increasing the relative humidity to greater than 95% for MUMPs devices was seen to lower the fatigue lifetimes at a given stress compared to behavior in ambient (30%–50% RH) air. Although scatter in the fatigue results and the logarithmic nature of the S/N plot tend to mask the effect, all data points for fatigue tests run in the 95% relative humidity environment lie on a different S/N curve below the curve acquired in ambient air (Fig. 3).

(4) No fatigue failures occurred under very high vacuum conditions ($\sim$25 °C, $<2.0\times10^{-7}$ mbar). All the samples tested *in vacuo* survived some 10^9-10^{10} cycles at high stresses without failure (in Fig. 3, these data points are plotted as run-outs, i.e., at the point where testing was stopped without failure). Moreover, no progressive fatigue damage accumulation or oxidation could be detected throughout these tests, as indicated by the lack of change in natural frequency of the device. This is in stark contrast to fatigue tests in air, where there was a continuous and progressive decay in the resonant frequency throughout the life.

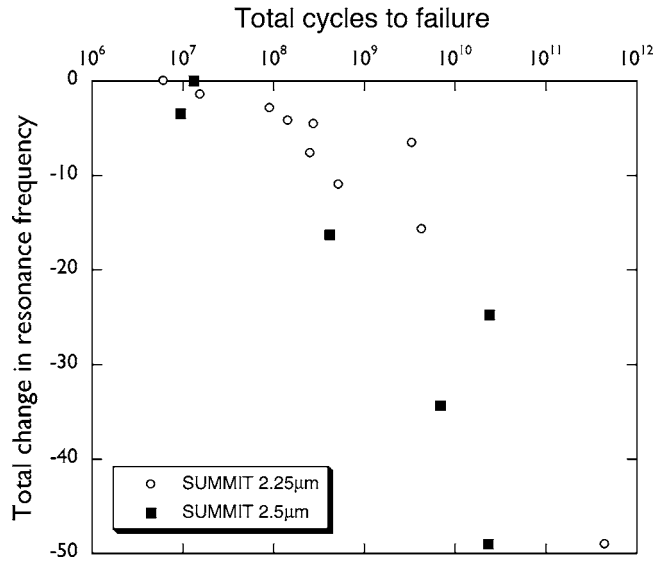

FIG. 5. The total resonance frequency decay (in Hz) at the point of failure for the two types of SUMMiT V™ devices (2.25 and 2.5 μm silicon structural device layer thickness) plotted vs the total number of cycles to failure. A (negative) second-order exponential trend can be observed between the total frequency decay and the number of cycles to failure.

B. TEM characterization

For the MUMPs devices, high-voltage TEM imaging of unthinned fatigue specimens revealed a local thickening of the oxide layer at the notch root. For specimens fatigued in ambient air, oxide layers as thick as 100 nm were measured [Fig. 6(b)]. Such local notch-root oxide thickening was not observed for mechanically fractured (non-fatigued) specimens in ambient air [Fig. 6(a)] nor for specimens fatigue cycled for up to 10^{10} cycles *in vacuo* [Fig. 6(c)]. In these latter two cases, the post-release oxides were found to be $\sim$15–30 nm thick, which is typical for the initial oxide thicknesses of MUMPs devices.[32,35]

The SUMMiT V™ devices have been processed to circumvent the galvanic effect associated with back-end-of-line metallization layers and consequently have a thinner post-release oxide than the MUMPs devices.[32] For the SUMMiT V™ devices, energy-filtered TEM oxygen maps of FIB samples revealed a similar trend in oxide thicknesses, although the overall magnitude of these layer thicknesses was much smaller than for the MUMPs devices. The initial oxide layer thickness away from the notch root and on freshly created fracture surfaces was between 3–6 nm in the SUMMiT V™ devices, and was locally thickened at the notch root up to about 15 nm after fatigue failure (Fig. 7). Interestingly, the oxide layer in locations where grain boundaries terminated at the surface did appear thicker up to $\sim$20 nm [Fig. 7(a)]. This could be due to higher local stresses associated with the geometry of the grain boundary in such locations or to faster oxidation rates at such sites of higher internal energy. In contrast, no oxide thickening was observed for devices cycled *in vacuo* (Fig. 8), i.e., in the absence of moisture and oxygen, consistent with the device resonance frequency measurements (described above) which showed no evidence of accumulated damage during these tests.

IV. DISCUSSION

The phenomenon of the time/cycle-delayed fatigue failure of micron-scale structural silicon films, an effect not seen in bulk silicon, is clearly an important failure mechanism that could limit the useful life of MEMS devices. In terms of traditional fatigue-crack growth mechanisms, which involve cyclic (e.g., dislocation) plasticity in ductile materials and a suppression of crack-tip (wake) shielding (e.g., crack bridging) in brittle materials,[25] the notion that a prototypical brittle material such as silicon fatigues at all is at first sight a mystery. We have proposed, however, that such very high-cycle,

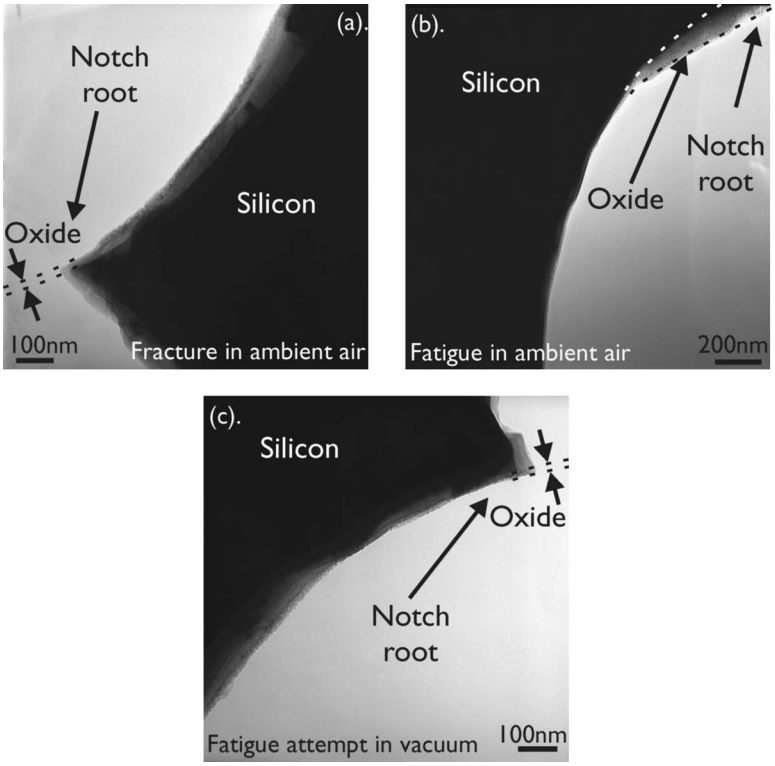

FIG. 6. High-voltage TEM (HVTEM) images from failed MUMPs resonator devices. (a) Monotonically fractured specimen in ambient air: no (local) oxide thickening. Because of sample tilt, some contrast in grains at the edge is visible. Only the top transparent part is amorphous. (b) Fatigued in ambient air with thickened oxide layer at the notch root (maximum cyclic stress at the notch root: 2.86 GPa; number of cycles at failure: 6.28×10^{8}). (c) Device after fatigue attempt *in vacuo* and subsequent single-cycle fracture: no oxide layer thickening (maximum cyclic stress at the notch root during fatigue attempt: 3.29 GPa, number of cycles when stopped: 1.14×10^{10}). Also in this case a contrast from grains on the edge is visible; only the top amorphous layer is oxide.

thin-film silicon fatigue is associated with a reaction-layer fatigue mechanism,[10–12] where the actual fracture processes occur not in the silicon itself but by the moisture-induced cracking in the cyclic stress-assisted thickened oxide layer. The stress/moisture-assisted cracking of the oxide layer, where hydroxyl ions in water react chemically with the SiO_2, destroying siloxane bonds,[41] induces stable crack growth which, provided the oxide layer is thick enough, results in a crack inside this layer large enough to exceed the critical crack size for the entire structure, whereupon the structure fails catastrophically. Both oxide thickening during cyclic fatigue loading and the presence of nanoscale stable cracks within the oxide layer of these films after cycling have been directly observed.[10,11] Similarly, Allameh *et al.*[18] report a surface roughening effect at stress concentrations during fatigue of micron-scale silicon (also reported by Bagdahn and Sharpe[22]), and have suggested a complementary mechanism involving stress-assisted oxide thickening, caused by dissolution of the surface oxide, which forms deep grooves in the vicinity of the notch that become sites for crack initiation.

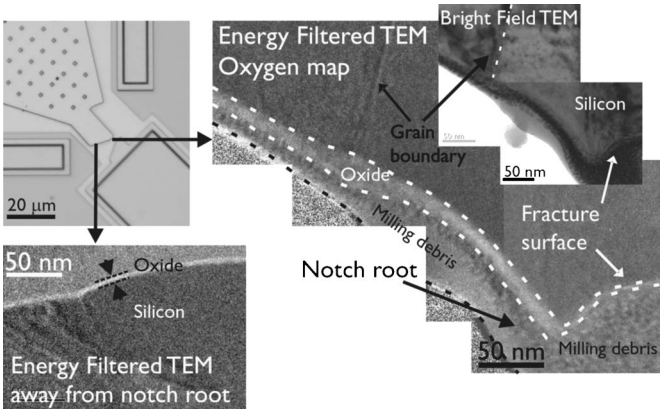

FIG. 7. Energy-filtered transmission electron microscopy (EFTEM) images of surface oxides following fatigue failure in ambient air of a SUMMiT V™ device, showing a thickened oxide around the notch root (15 nm) of up to 20 nm at a grain boundary terminating at the surface. Oxide layers of 3–5 nm have been observed away from the notch as well as on the freshly created fracture surface.

The precise mechanism by which the surface oxide thickens under the influence of cyclic stresses is yet unknown, but could be related to some form of stress-assisted diffusion or an increased oxidation reaction rate at the silicon/oxide interface. Compressive stresses occur in the silicon-oxide layer during oxidization because the molar volume of SiO_2 ($27\ cm^3/mol$) is larger than for Si ($12\ cm^3/mol$). The corresponding reduction in oxidation rate as a silicon-oxide layer grows thicker has been partly attributed to the presence of these stresses because of a decrease in oxidant diffusion rate.[42–44] Additionally, tensile stresses in the silicon caused by the oxide can cause the oxidation reaction at the silicon/oxide interface to occur more quickly.[45] When a cyclic load is applied, the compressive stresses in the oxide will be relieved during the tensile part of the loading cycle, which could result in less reduction in the oxidation reaction rate as the oxide grows thicker. Moreover, in combination with an applied compressive load in another part of the loading cycle, which increases the oxidation reaction, a rapid oxidation process could occur that results in the growth of thickened oxides in silicon at points of high cyclic stresses.

This reaction-layer model is consistent with the fact (i) that silicon fatigue is only seen in thin-film silicon, where a crack in the oxide layer can reach the critical size required to break the entire structure, and not in bulk silicon, where the critical crack size would be significantly larger than the ox-

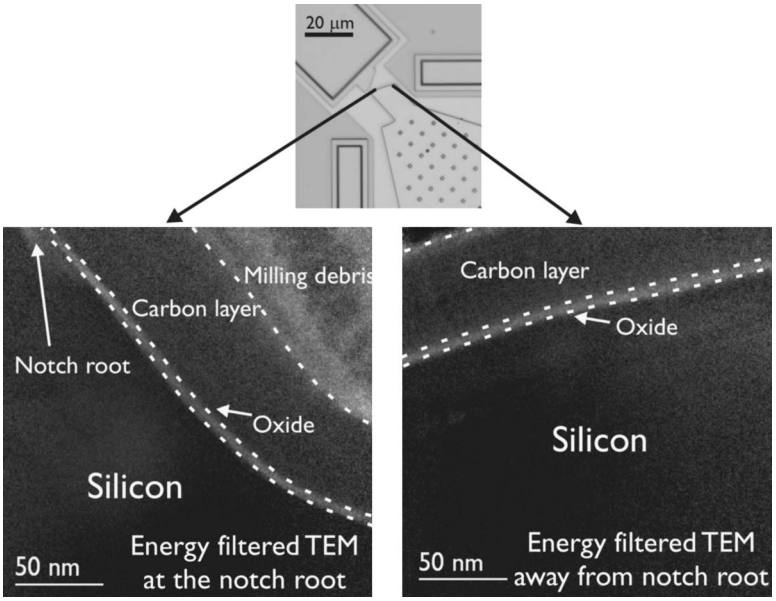

FIG. 8. EFTEM images of surface oxides of the surface oxide after fatigue cycling a SUMMIT™ device in very high vacuum ($P<2.0\times10^{-7}$ mbar), showing no local oxide thickening at the notch (left) in comparison with the oxide thickness away from the notch root of the same device (right). The oxide thickness for this device, which had a film thickness of 2.5 μm in both stressed and unstressed regions, was 5–6 nm. It was cycled for 6.7×10^{10} cycles at a maximum cyclic stress of 4.14 GPa without fatigue failure.

ide thickness, and (ii) that silica is highly prone to moisture-induced fracture: the silicon itself is not susceptible to either environmental cracking or fatigue.

The S/N results presented in Fig. 3 for different devices and environments, together with the damage accumulation data (decay in resonance frequency with cycles) in Figs. 4 and 5 and oxide layer thickness measurements in Figs. 6 and 7, provide a considerable body of experimental evidence to support the reaction-layer mechanism. Specifically, the S/N data clearly show that the thin-film silicon fatigue effect occurs in ambient air in devices with both small initial oxide layers, i.e., the SUMMiT V™ devices, as well as those with large oxide layers, i.e., from the MUMPs foundry, in this work from several fabrication runs. However, the SUMMiT V™ devices appear to be stronger, a trend consistent with the published tensile strength data for MUMPs and SUMMiT V™ polysilicon.[46,47] This higher strength translates into higher overall fatigue resistance (at a given applied maximum stress, the lifetimes of SUMMiT V™ devices were many orders of magnitude longer), presumably due to their thinner initial oxide films. We note that SUMMiT V™ devices fabricated from a 2.50 μm structural silicon layer (P21) have somewhat less fatigue resistance than those with a thinner (2.25 μm, P3) layer. This is partly associated with the fact that devices fabricated from a thicker silicon film have more sidewall surface area and hence have a higher probability of containing microflaws. This statistical size effect means that samples consisting of thicker layers may display a lower strength even if the material is nominally similar.[47,48] More importantly, the sidewall surface roughness of the two devices is different. The root mean square (rms) roughness of the P3 devices is ~90% of the rms roughness of the P21 devices.[47] This difference in roughness allows for larger microflaws in the P21 devices than in the P3 devices.

Accompanying TEM characterization of the amorphous silica layer after fatigue clearly shows that regardless of the starting oxide thickness, the oxide layer in the vicinity of the notch thickens by a factor of 4–6 times after $\sim10^{10}$ cycles in ambient or high-humidity air (Figs. 6 and 7). However, the maximum oxide thickness h varies substantially in devices with a different origin. Whereas notch-root oxides up to 100 nm thick were found in failed MUMPs devices, they were typically on the order of 20 nm thick in the SUMMiT V™ devices. Recently, Pierron and Muhlstein[49] have proposed that reaction-layer fatigue can occur in two different scenarios: (i) the crack can stably grow inside the oxide until it reaches the critical crack size a_c, i.e., the stress intensity for unstable crack propagation into the entire device is exceeded ($a_c \leqslant h$), or (ii) the crack can grow stably toward the silicon/oxide interface and change to unstable growth as it reaches this interface ($h=a_c$). In this second scenario the critical crack size is shorter than in the first scenario because of an additional driving force for unstable crack advancement as it reaches the silicon/oxide interface.[49] For the MUMPs devices that have relatively thick initial (post-release) oxides (~15–30 nm) which grow with cycling up to 100 nm, the first scenario applies because critical crack lengths of ~50 nm will be reached within the oxide before the crack reaches the interface.[46,49] The SUMMiT V™ devices, conversely, have thinner initial oxides (3–6 nm) which grow to a maximum of ~20 nm thick. Here unstable cracking can only commence when the crack reaches the silicon/oxide interface, which allows for reaction-layer mechanism to occur in oxide layers down to ~15 nm.[49] Note that in both of these fatigue scenarios the only crack growth occurring in the silicon is of an unstable nature, which is consistent with the notion that bulk silicon does not fatigue, but micron-scale silicon does.

One critical experimental observation was that cycling MUMPs devices in higher humidity environments, specifically 95% RH air, led to a definitive reduction in fatigue resistance in terms of shorter lifetimes (up to an order of magnitude) at a given applied stress, as compared to the behavior in ambient 30%–40% RH air (Fig. 3). This observation is again consistent with the reaction-layer mechanism as higher humidity would be expected to accelerate the stress-assisted oxidation and environmental cracking pro-

cesses, leading to earlier failures. Indeed, a recent study on single crystal silicon has shown that fatigue damage accumulation occurs more rapidly in higher relative humidity conditions.[50] More importantly, no fatigue failures were observed *in vacuo*, even after cycling at stresses close to the fracture stress for more than 10^{10} cycles (Fig. 3). During these experiments, no change in resonant frequency could be detected, indicating that neither substantial crack growth nor oxidation was occurring during these tests. Furthermore, TEM layer thickness measurements of the oxides in both MUMPs and SUMMiT V™ devices showed no local oxide thickening at points of high stress (Figs. 6 and 8). As minimizing the presence of oxygen and moisture in the test environment would act to suppress fatigue damage, i.e., oxidation and subcritical cracking in the oxide layer, these results are again fully consistent with the reaction-layer mechanism. It is also clear that the models for thin-film silicon fatigue based on mechanical (non-environmental) fatigue mechanisms,[14–16] are likely to be far less relevant.

V. CONCLUSIONS

Based on an experimental study of the very high-cycle fatigue ($\sim 10^6$–10^{12} cycles) of micron-scale polycrystalline silicon (freestanding) structural films (2–2.5 μm thick) from two different fabrication sources (MUMPs and SUMMiT V™), tested in ambient air ($\sim$25 °C, 30%–40% RH), high relative humidity air (>95% RH), and high vacuum ($>2 \times 10^{-7}$ mbar), the following conclusions can be made:

(1) In contrast to bulk silicon which is not susceptible to fatigue, high-frequency ($\sim$36–40 kHz) cyclic loading of micron-scale polysilicon thin films in room air (at a stress ratio of −1) resulted in premature fatigue failure after $\sim 10^6$–10^{12} cycles at applied maximum stresses less than the single-cycle fracture strength. Similar to previous studies, stress-life (S/N) curves were obtained, with lifetimes in excess of $\sim 10^{11}$ cycles being achieved when maximum stresses were typically $\sim$70% of the fracture strength.

(2) Such fatigue behavior in ambient air was observed in both MUMPs devices where the initial (post-release) oxide layers were large ($\sim$15–30 nm), and in SUMMiT V™ devices where the post-release oxide thicknesses were much smaller ($\sim$3–6 nm). At a given applied (maximum) stress, the lifetimes were many orders of magnitude longer in the higher-strength SUMMiT V™ polysilicon films.

(3) The fatigue behavior and hence the corresponding device lifetimes were highly sensitive to the test environment. The lifetimes were observed to be up to an order of magnitude shorter in a high-humidity atmosphere (>95% RH air), as compared to ambient air (30%–40% RH). No fatigue failures could be induced for tests run *in vacuo*, even after cycling at stresses close to the fracture stress for more than 10^{10} cycles.

(4) For both MUMPs and SUMMiT V™ devices, the cumulative fatigue damage, which has been related to local oxidation and subcritical cracking, could be detected throughout the fatigue life by a progressive decay in the resonant frequency of the device. Such behavior was always seen for tests in air, but never for tests *in vacuo* where no changes in resonance could be detected.

(5) High-voltage and energy-filtered transmission electron microscopy imaging of the silicon-oxide layers after cycling confirmed the occurrence of thickening of the oxide films, typically by four to six times, in the locally high stress region in the vicinity of the notch. The presence of nanoscale subcritical cracks was observed in these thickened oxide layers. Such behavior was not observed after cycling *in vacuo*.

(6) The presented fatigue results are consistent with the reaction-layer fatigue mechanism for the very high-cycle fatigue failure of micron-scale silicon films, where cyclic stress-induced delayed failures can occur at stresses less than the (single-cycle) fracture strength due to moisture-induced subcritical (stable) cracking within the oxide layer. The mechanism is specific to thin-film silicon where cracks within the oxide can reach a size large enough to cause catastrophic failure of the entire device.

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[1] M. J. Madou, *Fundamentals of Microfabrication*, 2nd ed. (CRC, Boca Raton, FL, 2002).
[2] N. Maluf and K. Williams, *An Introduction to Microelectromechanical Systems Engineering* (Artech House, Boston, 2004).
[3] A. D. Romig, Jr., M. T. Dugger, and P. J. McWhorter, Acta Mater. **51**, 5837 (2003).
[4] R. Maboudian, W. R. Ashurst, and C. Carraro, Tribol. Lett. **12**, 95 (2002).
[5] K. Komvopoulos, Wear **200**, 305 (1996).
[6] J. A. Connally and S. B. Brown, Science **256**, 1537 (1992).
[7] J. A. Connally and S. B. Brown, Exp. Mech. **33**, 81 (1993).
[8] C. L. Muhlstein, S. B. Brown, and R. O. Ritchie, J. Microelectromech. Syst. **10**, 593 (2001).
[9] C. L. Muhlstein, S. B. Brown, and R. O. Ritchie, Sens. Actuators, A **94**, 177 (2001).
[10] C. L. Muhlstein, E. A. Stach, and R. O. Ritchie, Appl. Phys. Lett. **80**, 1532 (2002).
[11] C. L. Muhlstein, E. A. Stach, and R. O. Ritchie, Acta Mater. **50**, 3579 (2002).
[12] D. H. Alsem, E. A. Stach, C. L. Muhlstein, and R. O. Ritchie, Appl. Phys. Lett. **86**, 041914 (2005).
[13] H. Kahn, R. Ballarini, R. L. Mullen, and A. H. Heuer, Proc. R. Soc.

London, Ser. A **455**, 3807 (1999).
[14]H. Kahn, R. Ballerini, J. J. Bellante, and A. H. Heuer, Science **298**, 1215 (2002).
[15]H. Kahn, R. Ballerini, A. H. Heuer, Curr. Opin. Solid State Mater. Sci. **8**, 71 (2004).
[16]H. Kahn, L. Chen, R. Ballerini, and A. H. Heuer, Acta Mater. **54**, 667 (2006).
[17]S. Allameh, B. Gally, S. B. Brown, and W. O. Soboyejo, Mater. Res. Soc. Symp. Proc. **657**, EE2.3.1 (2001).
[18]S. Allameh, P. Shrotriya, A. Butterwick, S. B. Brown, and W. O. Soboyejo, J. Microelectromech. Syst. **12**, 313 (2003).
[19]P. Shrotriya, S. Allameh, A. Butterwick, S. B. Brown, and W. O. Soboyejo, Mater. Res. Soc. Symp. Proc. **687**, B2.3.1 (2002).
[20]P. Shrotriya, S. Allameh, and W. O. Soboyejo, Mech. Mater. **36**, 35 (2004).
[21]W. N. Sharpe, J. Bagdahn, K. Jackson, and G. Coles, J. Mater. Sci. **38**, 4075 (2003).
[22]J. Bagdahn and W. N. Sharpe, Sens. Actuators, A **103**, 9 (2003).
[23]W. N. Sharpe and J. Bagdahn, Mech. Mater. **36**, 3 (2004).
[24]X. Li and B. Bhushan, Surf. Coat. Technol. **163–164**, 521 (2003).
[25]R. O. Ritchie, Int. J. Fract. **100**, 55 (1999).
[26]S. Suresh, *Fatigue of Materials*, 2nd ed. (Cambridge University Press, Cambridge, 1998).
[27]J. R. Brockenbrough and S. Suresh, J. Mech. Phys. Solids **35**, 721 (1987).
[28]O. N. Pierron and C. L. Muhlstein, Fatigue Fract. Eng. Mater. Struct. **30**, 57 (2007).
[29]S. Sundararajan and B. Bhushan, Sens. Actuators, A **101**, 338 (2002).
[30]T. Namazu and Y. Isono, Micro Electro Mechanical Systems, 2004. 17th IEEE International Conference on MEMS Technical Digest, 149 (2004).
[31]M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami, and M. Ohwada, J. Appl. Phys. **68**, 1272 (1990).
[32]O. N. Pierron, D. D. Macdonald, and C. L. Muhlstein, Appl. Phys. Lett. **86**, 211919 (2005).
[33]D. Koester, A. Cowen, R. Mahadevan, M. Stonefield, and B. Hardy, *PolyMUMPs Design Handbook* (MEMSCAP, Bernin, France, 2003), Rev. 10.
[34]More information on the MUMP at http://www.memscap.com/memsrus
[35]H. Kahn, C. Deeb, I. Chasiotis, and A. H. Heuer, J. Microelectromech. Syst. **14**, 914 (2005).
[36]More information on the SUMMiT V™ process at http://mems.sandia.gov
[37]W. W. Van Arsdell and S. B. Brown, J. Microelectromech. Syst. **8**, 319 (1999).
[38]J. J. Sniegowski and E. J. Garcia, Proc. SPIE **2383** 46 (1995).
[39]*Introduction to Focused Ion Beams: Instrumentation, Theory, Techniques and Practice*, edited by L. A. Giannuzzi and F. A. Stevie (Springer, New York, 2004).
[40]C. L. Muhlstein, R. T. Howe, and R. O. Ritchie, Mech. Mater. **36**, 13 (2004).
[41]S. M. Wiederhorn, J. Am. Ceram. Soc. **55** 81 (1972).
[42]A. Fargeix, G. Ghibaudo, and G. Kamarinos, J. Appl. Phys. **54**, 2878 (1983).
[43]A. Fargeix and G. Ghibaudo, J. Appl. Phys. **54**, 7153 (1983).
[44]A. Fargeix and G. Ghibaudo, J. Appl. Phys. **56**, 589 (1984).
[45]E. A. Irene, J. Appl. Phys. **54**, 5416 (1983).
[46]W. N. Sharpe, Jr., K. Jackson, G. Coles, and D. A. LaVan, Mater. Res. Soc. Symp. Proc. **657**, EE5.5.1 (2001).
[47]B. L. Boyce, J. M. Grazier, T. E. Buchheit, and M. J. Shaw, J. Microelectromech. Syst. (accepted).
[48]W. N. Sharpe, Jr., K. M. Jackson, K. J. Hemker, and Z. Xie, J. Microelectromech. Syst. **10**, 317 (2001).
[49]O. N. Pierron and C. L. Muhlstein, Int. J. Fract. **135**, 1 (2005).
[50]O. N. Pierron and C. L. Muhlstein, J. Microelectromech. Syst. **15**, 111 (2006).