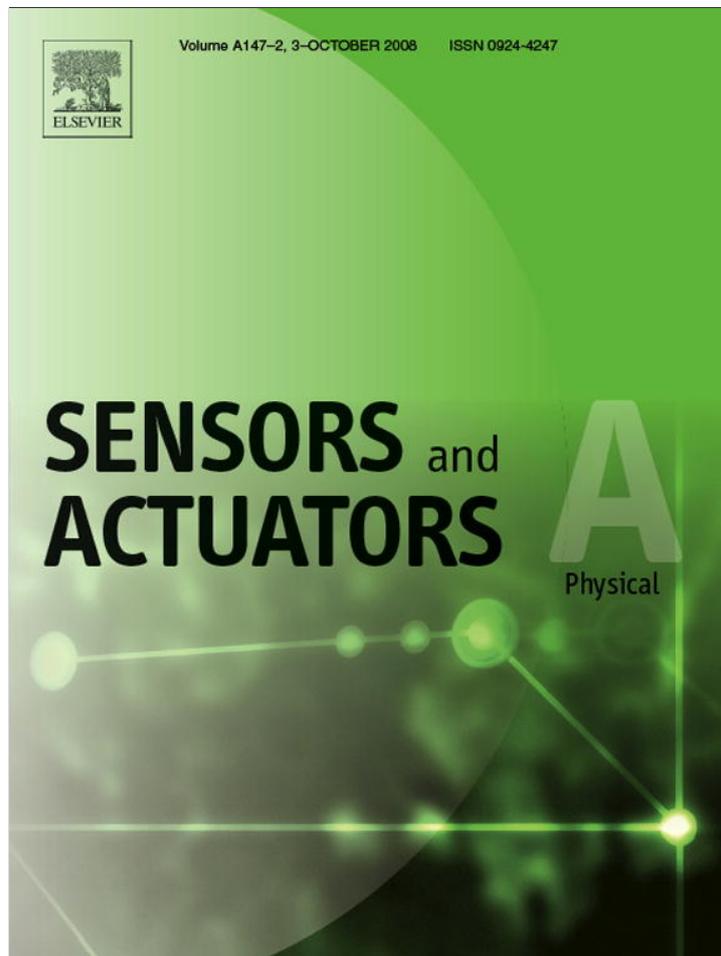


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# Effect of post-release sidewall morphology on the fracture and fatigue properties of polycrystalline silicon structural films

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## ARTICLE INFO

### Article history:

Received 22 February 2008

Received in revised form 29 May 2008

Accepted 30 May 2008

Available online 6 June 2008

### Keywords:

Polysilicon  
Silicon oxide  
Fracture  
Fatigue  
Thin films  
MEMS

## ABSTRACT

Surface properties can markedly affect the mechanical behavior of structural thin films used in microelectromechanical systems (MEMS) applications. This study highlights the striking difference in the sidewall surface morphology of  $n^+$ -type polysilicon films from two popular MEMS processes and its effect on fracture and fatigue properties. The sidewall surface roughness was measured using atomic force microscopy, whereas silicon oxide thickness and grain size were measured using (energy-filtered) transmission electron microscopy. These measurements show that the oxide layers are not always thin native oxides, as often assumed; moreover, the roughness of the silicon/silicon oxide interface is significantly influenced by the oxidation mechanism. Thick silicon oxides ( $20 \pm 5$  nm) found in PolyMUMPs™ films are caused by galvanic corrosion from the presence of gold on the chip, whereas in SUMMiT V™ films a much thinner ( $3.5 \pm 1.0$  nm) native oxide was observed. The thicker oxide layers, in combination with differences in sidewall roughness ( $14 \pm 5$  nm for PolyMUMPs™ and  $10 \pm 2$  nm for SUMMiT V™), can have a significant effect on the reliability of polysilicon structures subjecting to bending loads; this is shown by measurements of the fracture strength ( $3.8 \pm 0.3$  GPa for PolyMUMPs™ and  $4.8 \pm 0.2$  GPa for SUMMiT V™) and differences in the stress-lifetime cyclic fatigue behavior.

Published by Elsevier B.V.

## 1. Introduction

Because of their large surface to volume ratio, the surface properties of structural thin films used in microelectromechanical systems (MEMS) invariably have a significant effect on their material properties. Consequently, it is imperative to fully characterize the surfaces of the materials and components used in MEMS designs in order to correctly predict device behavior and reliability after fabrication. Such surface characterization is relevant to both the electrical and mechanical behavior of the MEMS device.

Since silicon is currently one of the main materials used in MEMS and many devices contain in-plane flexures [1], this study is focused on the influence of sidewall morphology and silicon oxide thicknesses on the mechanical properties – specifically strength

and cyclic fatigue resistance in bending – of micrometer-scale polycrystalline (polysilicon) structural films. Examples of how sidewall morphology and silicon oxide layers influence the mechanical behavior of silicon are numerous. One notable example is the friction and wear behavior of micrometer-scale polysilicon, which is strongly affected by roughness and surface oxide layers [2]. Specifically, for polysilicon in ambient air, the coefficient of friction for silicon and silicon oxide are quite different [3], and higher wear rates can be directly correlated with higher surface roughness [4]. Additionally, for thin films, the thickness of the silicon oxide layer and the sidewall roughness can affect fracture behavior [2,5–7]. As the fracture toughness of silicon ( $K_{IC} \sim 1$  MPa $\sqrt{m}$  [8,9]) is almost 20% higher than that of silicon oxide ( $K_{IC} \sim 0.85$  MPa $\sqrt{m}$  [10]), a thick oxide layer on a micrometer-scale silicon film can be quite embrittling; moreover, because fracture processes dominate the wear of silicon [11], these features will also influence wear behavior. More importantly, unlike (macro-scale) silicon [12–15], silicon oxide is susceptible to environmentally assisted subcritical cracking [16]. Such subcritical crack growth in SiO<sub>2</sub> occurs at stress intensities that are a factor of three or so lower than the critical stress intensity for

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failure (the fracture toughness), specifically above a threshold stress intensity factor of  $K_{TH} \sim 0.25 \text{ MPa}\sqrt{\text{m}}$  [17]. This latter phenomenon has been associated with observations that micrometer-scale structural films of silicon are susceptible to failure under high-cycle fatigue loading. Specifically, moisture-assisted subcritical cracking within a cyclic stress-assisted thickened oxide layer that becomes thick enough to accommodate critical crack sizes can result in catastrophic failure, a process that has been named “reaction-layer” fatigue [17–25].<sup>1</sup> These studies also revealed that the oxide thickness in post-release thin film silicon structures, rather than being only a few nanometers thick as is regularly assumed (e.g., [26,27]), can sometimes be significantly larger. Often the assumed thickness of this post-release oxide layer is derived from studies into native oxide growth on silicon wafers or on blanket films, which show that in ambient air the self-passivating silicon oxide layer thickness will indeed be several nanometers thick [26,28]. However, these measurements do not always apply to micrometer-scale polysilicon structural films [29,30].

In light of these studies, the present work is focused on an in-depth characterization of the sidewall surfaces of two frequently used multi-user MEMS processes: the MEMSCAP PolyMUMPs™ process and the Sandia National Laboratories SUMMiT V™ process. Scanning and transmission electron microscopy (respectively, SEM and TEM) is combined with atomic force microscopy (AFM) to characterize the polysilicon sidewall surface and silicon/silicon oxide interface, and to obtain sidewall surface roughness, silicon oxide thickness and in-plane grain size measurements. The effects of these parameters are illustrated by direct comparison of the fracture strength and fatigue resistance of polysilicon devices fabricated by these two different processes.

## 2. Experimental methods

Post-release sidewall surfaces from both the MEMSCAP PolyMUMPs™ and Sandia National Laboratories SUMMiT V™ n<sup>+</sup>-type polysilicon processes were examined. The PolyMUMPs™ devices studied had been 49% HF released according to the release process prescribed in the process manual for 3 min [33]. The SUMMiT V™ films that were used for SEM and AFM imaging had a perfluorodecyltrichlorosilane,  $\text{CF}_3(\text{CF}_2)_7(\text{CH}_2)_2\text{SiCl}_3$  (FDTS) monolayer coating deposited on them during the release procedure,<sup>2</sup> whereas the films used for the oxide thickness measurements and all measurements of fracture strength and fatigue endurance did not. Given the measured roughness values and conformal nature of the coating, the influence of this  $\sim 2 \text{ nm}$  thick monolayer coating and underlying silicon oxide [34] on SEM/AFM imaging was not deemed to be significant. The monolayer coating, however, does reduce the work of adhesion and friction coefficient of the contacting surfaces [4,35], thereby making transport, handling and operating of the devices easier. Further details of the process flows for the two polysilicon fabrication processes can be found in Refs. [33,36,37].

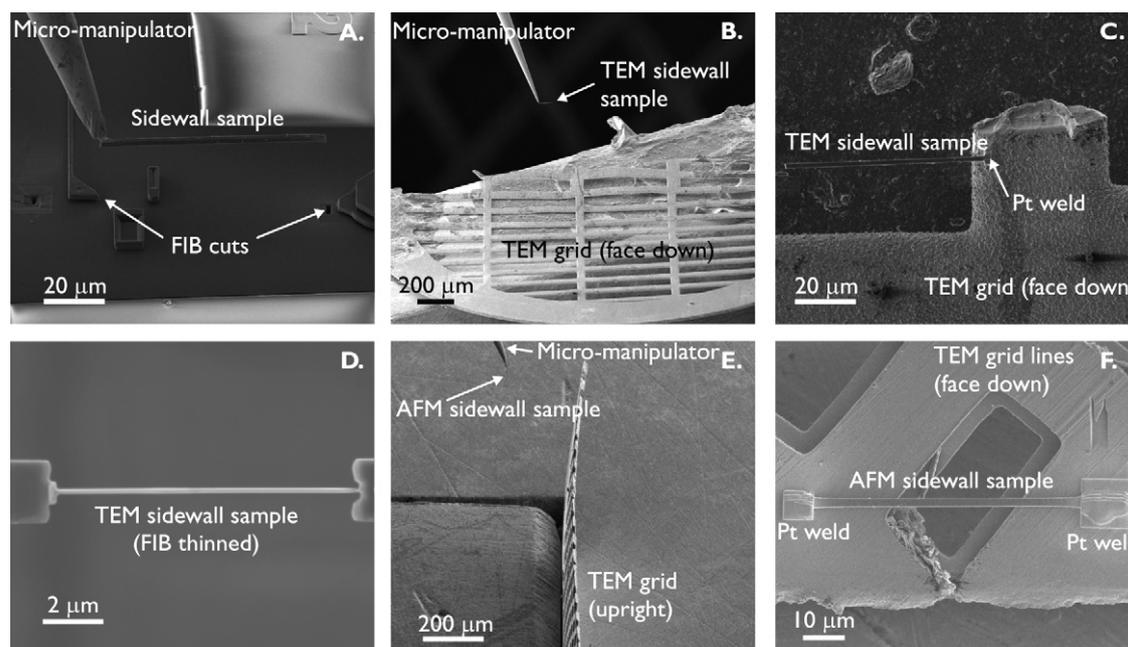
As noted above, SEM, TEM and AFM were used to characterize the morphology of the sidewall surfaces and oxides. Specifically,

TEM and AFM samples were prepared using focused-ion beam (FIB) lift-out sample preparation techniques (FEI Strata DB235 Dual Beam FIB equipped with an OmniProbe™ micro-manipulator), as illustrated in Fig. 1 [4,11,33]. First, the sidewall sample of interest was cut out of the MEMS device and attached to the micro-manipulator using Pt deposited by the ion beam (Fig. 1A). To prepare a TEM specimen, the sidewall sample was transferred to half a copper TEM grid face-up (Fig. 1B), whereas for an AFM specimen the sidewall sample was attached to an upright TEM grid (Fig. 1E). To finish the AFM specimen, the TEM grid was put down face-up, such that the sidewall was face up. To finish the TEM specimen, a thin carbon coating was sputtered onto its surface to better demark the oxide from any re-deposited milling debris, and then thinned using the ion beam to make it electron transparent. All TEM samples were thinned to about 150 nm (with the cross-sections taken halfway between the top and bottom of the film) after depositing a protective layer of platinum on the surface on the side for thinning where the ion beam impinges. After thinning there was invariably some re-deposited milling debris attached to the side of the specimen that was not protected by the platinum deposit; such debris, which was separated from the oxide layers by the sputtered carbon layer, however, did not appear to alter the surface conditions. SEM imaging was carried out using a FEI Strata DB235 Dual Beam FIB at 5 kV. TEM imaging was performed in both a 300 kV JEOL 3010 (LaB<sub>6</sub> filament) and Philips CM200-FEG (Field Emission Gun), operated at 200 keV, with a Gatan Image Filter (GIF) system. This GIF allows energy-filtered imaging to create an elemental (in this case, oxygen) map of an area of interest (so-called energy-filtered transmission electron microscopy, or EFTEM). The AFM measurements were performed using an Asylum Research MFP-3D instrument in non-contact mode. The root mean square (RMS) roughness of the sidewall surfaces was measured in sample areas of roughly  $4 \mu\text{m}^2$  and then averaged over a number of measurements (19 for PolyMUMPs™ and 12 for SUMMiT V™).

Fracture strength and fatigue experiments were performed using electrostatically actuated resonator devices without monolayer coatings, as described in refs. [24,38]. The device consists of a  $\sim 300 \mu\text{m}$  sided triangularly shaped free-standing proof mass connected to an anchor on the substrate by a notched cantilever beam. The mass is electrostatically driven in-plane at resonance (resonance frequency 36–40 kHz) with fully reversed loading (ratio of minimum to maximum stress,  $R = -1$ ) by an interdigitated comb drive at one side of the device, whereas the comb structure on the other side of the proof mass is used to capacitively sense the displacement of the device during operation using custom built electronics, filtering the output signal of the sense comb drive using an adjustable bandpass filter and converting this output current into a voltage that is input into a computer system running LABVIEW [24]. Using the measured (optically calibrated) displacement and finite-element calculation methods (ANSYS 5.7), the stress at the notch in the cantilever beam during the test can be readily calculated and plotted as a function of the number of cycles to failure to give a stress-lifetime fatigue curve [24]. The fatigue experiments shown here were all conducted in ambient air at room temperature (25 °C, 30–40% relative humidity). Corresponding fracture strength experiments were carried out by quickly following the resonance curve of the structures by rapidly increasing the driving frequency with a high applied driving voltage up to fracture. In order to mitigate any effect of the cyclic actuation and environmental decay of the structure, all fracture strength tests were operated at room temperature (25 °C) in a high vacuum (i.e., at pressures less than  $2.0 \times 10^{-7} \text{ mbar}$ ), which prevented the occurrence of any damage from environmentally assisted subcritical cracking [20,24].

<sup>1</sup> It should be noted that the mechanisms associated with the fatigue of silicon thin films is still the subject of some debate. For a more in-depth discussion, the reader is referred to the following reviews and viewpoint papers in Refs. [23,25,31,32].

<sup>2</sup> The coating was applied during the release procedure via the following steps in solution at room temperature: release etched (HF:HCL for 90 min), rinsed with deionized (DI) water, oxidized with H<sub>2</sub>O<sub>2</sub>, rinsed with DI water, transferred to isopropyl alcohol and then to iso-octane, transferred to 1 mM solution of the monolayer in iso-octane and held in solution for 2 h, transferred to neat iso-octane, then to isopropyl alcohol and to DI water, before finally being removed from DI water and air dried on class 10 clean bench.



**Fig. 1.** FIB sample preparation for TEM and AFM for a SUMMiT V™ polysilicon beam. (A) Sidewall sample attached to micromanipulator after being cut from the MEMS device. (B) and (C) Sidewall sample is transferred to half of a copper TEM grid and Pt welded into place (top of the beam facing upwards in (C)). (D) TEM specimen FIB thinned to electron transparency. (E) After cutting from device (A) the sidewall sample is attached to an upright TEM grid. (F) Final AFM specimen after putting grid face down and fortifying Pt welds (sidewall of beam facing upwards in (F)). After [4,11].

### 3. Results

#### 3.1. Grain size and sidewall roughness

The sidewall morphology of polysilicon films from both the PolyMUMPs™ and SUMMiT V™ process are shown, respectively, in Figs. 2A and 3A. On both sidewalls, vertical etch striations can be seen that reveal the morphology of the columnar grains through the films. The striations appear to have a larger periodicity on the SUMMiT V™ sidewalls than on the PolyMUMPs™ sidewalls, which is indicative of the formers larger grain size; additionally, the SUMMiT V™ etch striations appear to deviate significantly from running perfectly vertical, suggesting that the grain diameter at the top and bottom of the film are slightly different. Actual grain sizes, quantified using the linear intercept method [39] from cross-sectional TEM views from the middle of the films (Figs. 2B and 3B), gave values for the PolyMUMPs™ films of  $349 \pm 23$  nm, as compared to  $435 \pm 35$  nm for the SUMMiT V™ films. The cross-sections showed that both films were relatively dislocation-free, although there was ample evidence of twinning in both type of films, as indicated by arrows in Figs. 2B and 3B. Both type of films were measured (by SEM) to be of similar thickness; the PolyMUMPs™ film (Fig. 2) had a measured thickness of  $2.0 \pm 0.2$   $\mu\text{m}$ , whereas the SUMMiT V™ film (Fig. 3) had a measured film thickness<sup>3</sup> of  $2.2 \pm 0.2$   $\mu\text{m}$ . The PolyMUMPs™ sidewalls were found to be rougher with significantly more scatter in the measured roughness values. Specifically, AFM scans revealed an average RMS roughness of the surfaces of  $14 \pm 5$  nm for these films, as compared to  $10 \pm 2$  nm for the SUMMiT V™ films; this comparison has a 99.6% probability of being statistically significant, as determined by an unpaired Student's *t*-test (two-tailed distribution).

<sup>3</sup> Whereas the polysilicon layers from the PolyMUMPs™ samples were fabricated from the "Poly1" layer, the polysilicon layer from the SUMMiT V™ process that was investigated here was a stack of layers of "Poly1" and "Poly2".

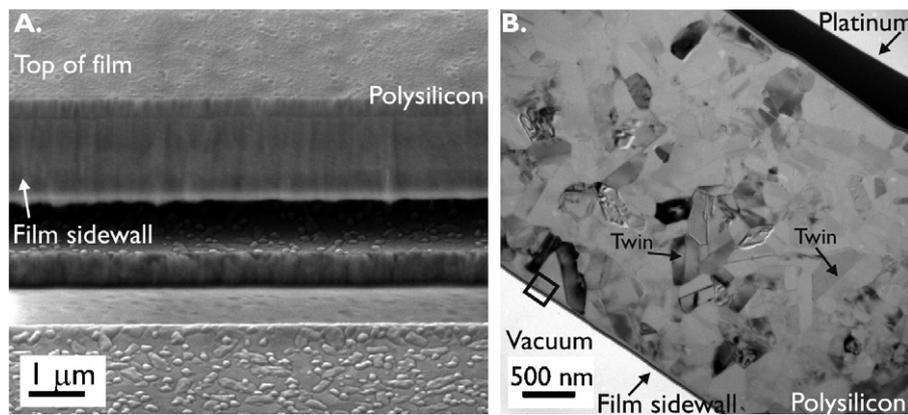
#### 3.2. Oxide thickness and Si/SiO<sub>2</sub> interface

The morphologies of the oxide layer and the silicon/silicon oxide interface in the sidewalls of the PolyMUMPs™ and SUMMiT V™ polysilicon films are shown respectively in Figs. 4 and 5 in the form of typical high-magnification bright-field TEM images and EFTEM images of the oxygen distribution at the surface. The exact thickness of the oxide film cannot be simply deduced from the bright field TEM images (Figs. 4A and 5A), mainly because of the presence of the 'milling debris' which like the oxide layer has an amorphous structure. However, the EFTEM images (Figs. 4B and 5B), which show oxygen maps of exactly the same regions, do clearly delineate the regions of silicon oxide.

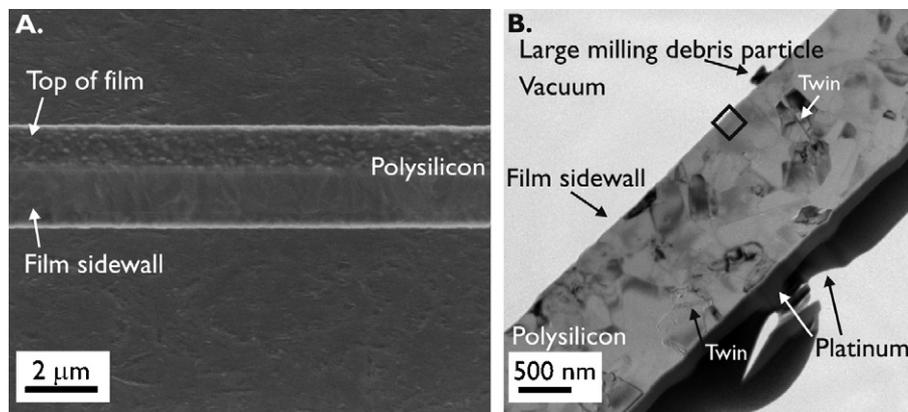
The silicon oxide layers in the SUMMiT V™ films (Fig. 4B) were  $3.5 \pm 1.0$  nm in thickness. In contrast, the oxide layers on the PolyMUMPs™ films (Fig. 5B) were some three to five times thicker ( $20 \pm 5$  nm in thickness), with a much rougher Si/SiO<sub>2</sub> interface (Figs. 4B and 5B); specifically, the amplitude of the waviness of the Si/SiO<sub>2</sub> interface is similar, but the wavelength of this waviness is shorter and a superposed finer scale roughness is visible for the PolyMUMPs™ films.

#### 3.3. Mechanical properties

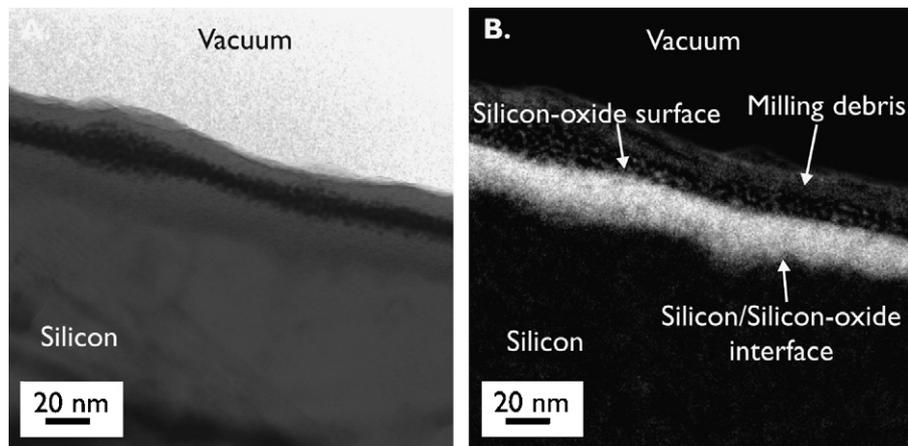
To illustrate how the sidewall morphology of polysilicon can influence its mechanical properties, results of fracture strength and fatigue lifetime tests for both PolyMUMPs™ and SUMMiT V™ devices are given in Fig. 6 and Table 1, together with their quantitative sidewall parameters. The measured fracture strength of the SUMMiT V™ devices is some 26% higher than for the PolyMUMPs™ devices (respectively  $3.8 \pm 0.3$  GPa and  $4.8 \pm 0.2$  GPa). Similarly, the fatigue resistance of the SUMMiT V™ devices [24] is also higher than for the PolyMUMPs™ devices, the former not only having a higher single-cycle fracture strength, but also a more shallow slope in the high-cycle regime of the stress-lifetime plot (Fig. 6). This results in a  $10^{10}$ -cycle fatigue endurance strength of the



**Fig. 2.** (A) PolyMUMPs™ SEM sidewall surface as seen from a 52 degree angle of incidence and (B) TEM cross-section as seen from the top of the film, along the axis of the in-plane grains. Examples of twin boundaries are marked, as well as the vacuum in the TEM column. The orientation of the images in Fig. 4 is marked with a square.



**Fig. 3.** (A) SUMMiT V™ SEM sidewall surface as seen from a 52 degrees angle of incidence and (B) TEM cross-section as seen from the top of the film, along the axis of the in-plane grains. Examples of twin boundaries are marked, as well as the vacuum in the TEM column. The orientation of the images in Fig. 5 is marked with a square.



**Fig. 4.** PolyMUMPs™ oxide morphology: (A) bright field TEM (B) EFTEM oxygen map showing silicon-oxide (thickness: 15–25 nm). The edge of the sample is marked by the vacuum in the TEM column.

**Table 1**

Summary of the sidewall morphology, structure, fracture strength and fatigue endurance of polysilicon films from the PolyMUMPs™ and SUMMiT V™ processes

	Grain size (nm)	RMS roughness (nm)	Oxide thickness (nm)	Fracture strength (GPa)	Fatigue endurance strength (10 <sup>10</sup> cycles) (GPa)
PolyMUMPs™	349 ± 23	14 ± 5	20 ± 5	3.8 ± 0.3	2.6 ± 0.3
SUMMiT V™	435 ± 35	10 ± 2	3.5 ± 1.0	4.8 ± 0.2	4.0 ± 0.2

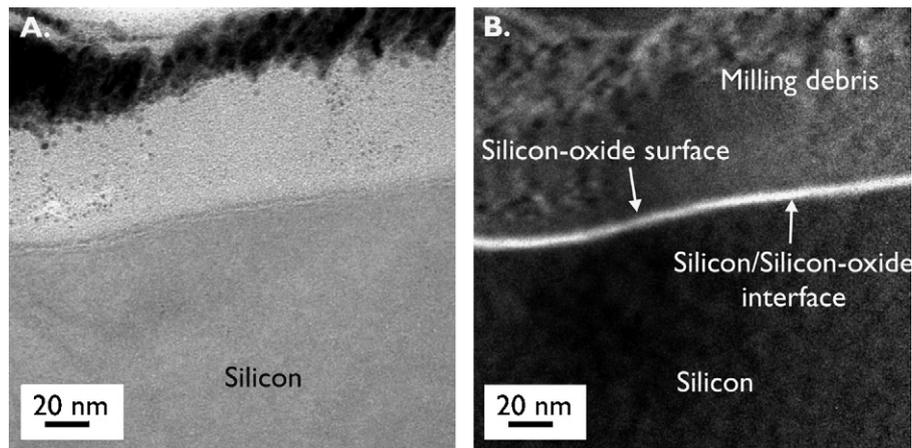


Fig. 5. SUMMiT V™ oxide morphology: (A) bright field TEM (B) EFTM oxygen map showing silicon-oxide (thickness: 2.5–4.5 nm).

PolyMUMPs™ films that is  $\sim 35\%$  lower than for the SUMMiT V™ films, *i.e.*,  $2.6 \pm 0.3$  GPa, as compared to  $4.0 \pm 0.2$  GPa. The locations of crack initiation were predominantly on the sidewall. This is indicated in Fig. 7 which shows typical fracture surfaces from fractured specimens of both the PolyMUMPs™ and SUMMiT V™ devices; river markings on the cleavage facets close to the notch root can be seen to trace back to fracture origin sites along the sidewalls.

#### 4. Discussion

The surfaces properties of structural thin polysilicon films are known to have a significant effect on their material properties. Since many micrometer-scale polysilicon devices contain in-plane flexures, the sidewall morphology, the silicon oxide thickness and their influence on the mechanical properties of polysilicon are clearly of importance; accordingly, their effect on strength and fatigue resistance was specifically investigated in this work.

##### 4.1. Polysilicon morphology

The measured difference in sidewall surface oxide thickness and Si/SiO<sub>2</sub> interface morphology between both fabrication processes (Figs. 4B and 5B and Table 1) can be attributed to the different physical/chemical mechanisms that lead to the formation of the oxide during the two fabrication processes. In the case of the SUMMiT

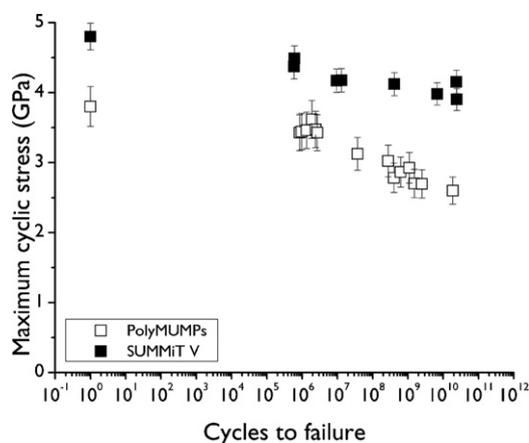
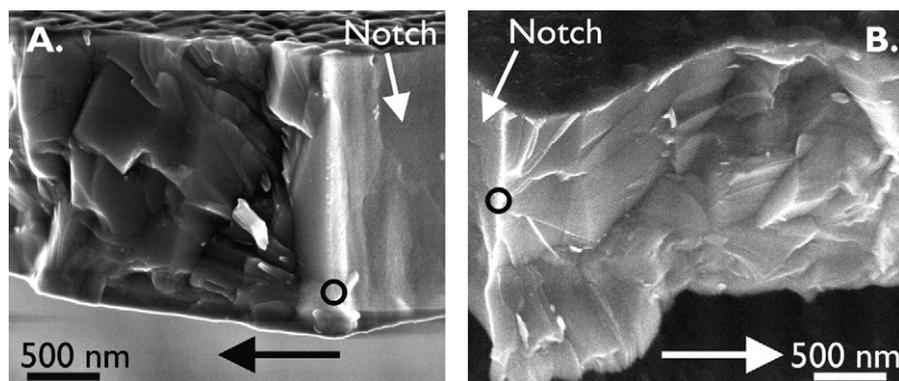


Fig. 6. Fracture strength (at 1 cycle to failure) and high-cycle fatigue lifetime ( $>10^5$  cycles to failure) in ambient air for PolyMUMPs™ and SUMMiT V™ fatigue resonator devices.

V™ structures, a post-release native oxide is known to grow and then self-passivate after several nanometers of growth; this is a well-established mechanism [26,28]. The much thicker oxide layers on the PolyMUMPs™ films are now known to be associated with a galvanic corrosion process during the HF release step [29,30]. Specifically, the PolyMUMPs™ process has a gold deposition step, mostly used to coat wire contact pads; the galvanic coupling between the heavily doped  $n^+$ -type polysilicon and the highly cathodic gold contact causes the growth of thick post-release oxides [29,30], which can typically reach thicknesses of up to 20 nm or more using standard PolyMUMPs™ release procedures [20,30]. It is shown here that this rapid oxidation at room temperature not only leads to a rougher Si/SiO<sub>2</sub> interface (Figs. 4B and 5B), but also contributes, together with inherent film properties like grain size, to a higher sidewall surface roughness (Table 1). It should be noted that the duration of the HF release step, the distance from the sidewall sample on the chip to the gold-coated areas, and the relative surface area of gold to polysilicon can all influence the oxide thickness [2,30].<sup>4</sup> Similarly, other differences in polysilicon film morphology between the two processes can be explained by differences in processing conditions. Although both processes use low-pressure chemical-vapor deposited (LPCVD) polysilicon films, followed by subsequent annealing steps, and are patterned using reactive-ion etching (RIE), the SUMMiT V™ polysilicon is phosphorous-doped during film deposition, while for the PolyMUMPs™ process the phosphorous is diffused into the polysilicon from sacrificial phosphosilicate glass (PSG) layers during the annealing steps [33,40]. This difference in doping method can have an important effect on the stress-state in the film and thus on the grain size [40], which affects the surface roughness. The larger grain size of the SUMMiT V™ films can be contributed to the differences between doping methods; additionally, SUMMiT V™ films are subjected to more high-temperature processing steps after deposition of the particular layers studied here. Because of longer annealing times, the grains have more time to grow to a larger lower energy configuration. This difference in grain size in turn affects the roughness of the sidewalls; grain boundaries etch more readily during patterning of the film, resulting in deeper grooves at grain boundaries [41], and larger grain size will result into a lower number of grain boundaries per unit sidewall length, therefore lowering the sidewall roughness. The larger grain size of the SUMMiT V™ devices is

<sup>4</sup> For the PolyMUMPs™ devices in this study the chips were released in 49% HF for 3 min; in the area of fatigue test devices the ratio of gold to polysilicon area is estimated to be 1:5.



**Fig. 7.** Examples of fracture surfaces of fractured devices from the PolyMUMPs™ (A) and SUMMiT V™ (B) processes showing probable initiation points (marked with a circle) at the notch sidewall. The horizontal arrows indicate the direction of crack propagation.

consistent with their lower measured sidewall surface roughness, as compared to the PolyMUMPs™ devices (Table 1).

#### 4.2. Polysilicon morphology and fracture, fatigue properties

We ascribe differences in the fracture and fatigue behavior of the two types of devices to the effect of the sidewall morphology; however, for this to be meaningful, it is important to verify that the failure origin of the specimens is actually on the sidewalls. The RMS roughness of the top surface for the SUMMiT V™ films is in the order of  $3.5 \pm 2.1$  [42] and for the PolyMUMPs™ films it is  $13 \pm 1$  nm [43,44]. The roughness of the SUMMiT V™ films is significantly lower than the sidewall roughness ( $10 \pm 2$  nm), whereas the PolyMUMPs™ has a top roughness that is similar to the sidewall roughness ( $14 \pm 5$  nm). Additionally, the top of the PolyMUMPs™ films have deeper and sharper grain boundary cusps than the sidewall [45,46]. This could result in a potentially important contribution of the morphology of the top of the film in the case for the PolyMUMPs™ specimen. However, since these tests are conducted in in-plane bending, the sidewall area is one of the regions on the device subjected to the highest stresses, and thus there is a larger probability of a pre-existing defect initiating a fracture there. In addition, the small top film surface area that is under high stress will be less constrained than most of the sidewall, leading to stress relaxation there. Moreover, as noted above, river markings on the cleavage facets on the fracture surfaces close to the notch root all strongly imply fracture initiation at the sidewall (Fig. 7). Specifically, the fracture surfaces for the PolyMUMPs™ devices (Fig. 7A) show failure initiation at sidewalls or at the intersection of the sidewalls and the top/bottom of the film; corresponding fracture initiation in the SUMMiT V™ devices (Fig. 7B) occurred mostly at the sidewall. These observations are consistent with the published roughness data of the top of the films [42–44] and published observations on fracture origin in PolyMUMPs™ tensile tests [47].

In general, the measured difference in fracture strength between the PolyMUMPs™ and the SUMMiT V™ devices (Fig. 6 and Table 1) can be related to two morphological factors: the sidewall roughness and the oxide layer thickness. As discussed above, as silicon oxide has a lower fracture toughness than silicon (*i.e.*,  $\sim 0.85$  MPa $\sqrt{m}$  vs.  $1.0$  MPa $\sqrt{m}$  [4–6]), this translates in micrometer-sized structural films to critical crack sizes (for catastrophic failure) that are typically up to tens of nanometers long [48]. Correspondingly, the presence of a  $\sim 20$ -nm thick oxide layer (instead of a  $\sim 3.5$  nm native post-release oxide) can negatively affect the fracture resistance. More importantly, the higher sidewall roughness for PolyMUMPs™ ( $14 \pm 5$  nm vs.  $10 \pm 2$  nm for SUMMiT V™, Table 1) and the addi-

tional effect of the roughness at the top of the film contributes to its lower fracture strength, as this can be directly related to the presence of larger surface flaws in the material [41], and hence lower stresses to fracture the specimens. This observation is consistent with a recently published study on the tensile strength of the different polysilicon layers of the SUMMiT V™ process, where the apparent strength of the different layers is degraded by the higher surface roughness [5]. This marked dependence on the roughness (and hence on a higher preponderance of flaws in the device) is reflected by the fact that although the fracture strength of polysilicon changes with different film microstructures, the fracture toughness of thin-film polysilicon is essentially totally independent of microstructure<sup>5</sup> (with  $K_{IC}$ ,  $\sim 1$  MPa $\sqrt{m}$ ) [49].

In addition to the observed roughness and oxide thickness effect on fracture strength, the effect of different oxide layer thicknesses is seen more clearly in high-cycle fatigue behavior of these two types of polysilicon specimens (Fig. 6) [24]. With a possibility of cyclic stress-assisted (moisture-induced) subcritical cracking occurring in the oxide layer, which is the mechanism for high-cycle fatigue of micrometer-scale silicon, the initial oxide layer thickness becomes a critical parameter; thicker initial oxides cause the devices to fail earlier because the oxide does not have to grow so much in order to reach the thickness needed to accommodate the critical crack sizes. Indeed, such a marked difference in fatigue resistance due to different silicon oxide layer thicknesses has indeed been observed (Fig. 6) [24]. For PolyMUMPs™ devices the fatigue resistance is significantly lower than for SUMMiT V™; this is apparent from the observed steeper slopes in the stress-lifetime fatigue data for PolyMUMPs™ samples. This effect, in combination with the lower single-cycle fracture strength, results in a  $10^{10}$ -cycle fatigue endurance strength of the PolyMUMPs™ films that is  $\sim 35\%$  lower than for the SUMMiT V™ films, *i.e.*,  $2.6 \pm 0.3$  GPa, as compared to  $4.0 \pm 0.2$  GPa. These results are consistent with the fact that polysilicon from the SUMMiT V™ process has a thinner post-release oxide ( $\sim 3.5$  nm vs.  $\sim 20$  nm for the PolyMUMPs™).

These fracture and fatigue results illustrate clearly the importance of the side-wall morphology on mechanical behavior of polysilicon structural films. Consequently, it is essential that sidewall parameters (including the oxide thickness) should be carefully considered when designing polysilicon MEMS devices,

<sup>5</sup> With fracture mechanics measurements, such as the fracture toughness, the onset of fracture is determined in a sample containing a worst-case crack, *e.g.*, a fatigue pre-crack. Unlike measurements of strength, which are invariably performed on smooth samples that are neither notched nor pre-cracked, such toughness measurements are thus much less dependent on the presence of flaws in the structure, unless they happen to be larger than the pre-crack in the sample.

estimating their reliability, and interpreting failure modes for polysilicon MEMS.

## 5. Conclusions

The intent of this study has been to show how the sidewall surface morphology, specifically the surface roughness and silicon oxide layer thickness, of n<sup>+</sup>-type polysilicon structural films can affect mechanical properties. Specifically, sidewalls of structures from two frequently used MEMS processes, PolyMUMPs™ and SUMMIT V™, were characterized and related to the measured fracture strength and cyclic fatigue resistance. Atomic force microscopy and (energy-filtered) transmission electron microscopy measurements were used to quantify the sidewall surface roughness and oxide thicknesses as well as the in-plane grain size. These measurements show that the post-release silicon oxides in MEMS processed devices can be much thicker than the few nanometers thick native oxide that is often assumed; moreover, the roughness of the silicon/silicon oxide interface is markedly influenced by the oxidation mechanism, with the faster oxidation process leading to thicker oxides and a consequent rougher interface. Both factors can significantly affect mechanical properties, in particular the damage-tolerant properties, of the films. This naturally affects the mechanical reliability of polysilicon structures manufactured from these films. The specific conclusions from this study are:

1. Thick ( $20 \pm 5$  nm) silicon oxide layers, associated with galvanic corrosion during the HF release step due to the presence of gold on the chip, were found in the PolyMUMPs™ polysilicon films, in contrast to the thin ( $3.5 \pm 1.0$  nm) native oxide layers in the SUMMIT V™ films.
2. Together with the in-plane grain size, thicker oxide layers in the PolyMUMPs™ films were associated with increased surface roughness of the sidewalls and with increased roughness at the Si/SiO<sub>2</sub> interface. The PolyMUMPs™ films displayed a surface roughness of  $14 \pm 5$  nm, as compared to  $10 \pm 2$  nm for the SUMMIT V™ films.
3. Due to their fivefold thicker oxides, 40% rougher sidewalls and roughness of the top of the film, measured fracture strengths for the PolyMUMPs™ films were over 20% lower than for the SUMMIT V™ films, i.e.,  $3.8 \pm 0.3$  GPa, as compared to  $4.8 \pm 0.2$  GPa.
4. Similarly, the thicker oxides and lower fracture strengths of the PolyMUMPs™ films resulted in an increased susceptibility of these films to cyclic fatigue failure, which are believed to fail by environmentally assisted subcritical cracking in a cyclic-stress assisted thickened silicon oxide. Specifically, the 10<sup>10</sup>-cycle fatigue endurance strength of the PolyMUMPs™ films was ~35% lower than for the SUMMIT V™ films, i.e.,  $2.6 \pm 0.3$  GPa, as compared to  $4.0 \pm 0.2$  GPa.

## Acknowledgements

This work was funded by the Director, Office of Science, Office of Basic Energy Sciences, Division of Materials Sciences and Engineering, of the U.S. Department of Energy under Contract no. DE-AC02-05CH11231 at the Lawrence Berkeley National Laboratory (LBNL). The authors acknowledge Drs. S. Timpe, K. Komvopoulos and M.T. Dugger for supplying devices for additional characterization, the use of the Molecular Foundry, specifically the assistance of Drs. P.D. Ashby and D.F. Ogletree with the AFM training, and the staff and facilities at the National Center for Electron Microscopy, both operated at LBNL with the support of the U.S. Department of Energy under Contract no. DE-AC02-05CH11231. Support for BLB is also gratefully acknowledged from Sandia National Laboratories, which is a multi-program laboratory operated by Sandia Corpo-

ration, a Lockheed-Martin Company, for the U.S. Department of Energy's National Nuclear Security Administration under Contract no. DE-AC04-94AL85000.

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